11.5 A 5GHz Resistive-Feedback CMOS LNA for Low-Cost Multi-Standard Applications

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Modern CMOS technology has excellent RF performance for applications below 10GHz. Some of this excess performance can be traded for smaller die size and process simplicity, making high-performance RF circuits compatible with digital CMOS technology. Such circuits are important for low-cost, highly integrated communication products, and for multi-standard systems with many radios. In this paper, we describe a 5GHz resistive-feedback LNA with a 2dB NF and 25dB of gain, occupying .025mm^2 of die area in 90nm CMOS technology.

Others have reported resistive-feedback broadband LNAs [1-3], but we improve the NF and return loss through a combination of technology and circuit design. Figure 11.5.1 is a simplified schematic diagram of the LNA. It consists of a g_m-enhanced cascode amplifier M_1-M_2 with source follower feedback buffer M_3. This arrangement results in M_1 and M_2 both having a voltage gain of ~13dB. C_{PFB} compensates for parasitic capacitance C_L and increases the bandwidth. Feedback resistor R_F is DC blocked by C_2. DC bias is provided by a feedback level-shifting source follower circuit (not shown) and isolating resistors R_1 and R_2. This biasing circuit has little impact on AC performance. M_4 is a separate source follower, which would typically form the transconductor in a mixer with R_M when I_{OUT} is taken from its drain. In our case, M_4 interfaces to a 50Ω driver for testing and provides additional reverse isolation.

Input matching at moderate frequencies is set according to

$$R_{in} \cong \frac{R_F}{1+A_V} \cong \frac{R_F}{A_V}. \quad (1)$$

For $R_F \cong 1K\Omega$ and $A_V \cong 20$, $R_{in} \cong 50\Omega$. Matching can be enhanced with off-chip input inductance, such as a bond wire, and/or properly sizing R_L, M_3 and I_3 as explained below. It is well known that the input impedance of the source of M_3 is inductive, given by

$$L_{EQ} \cong C_{gs3}\frac{R_L}{g_{m3}} = \frac{R_L}{2\pi f_{t3}}, \quad (2)$$

where the subscript 3 denotes parameters for M_3. C_2 has a 3% parasitic capacitance to substrate on each side and L_{EQ} can be chosen to resonate with this parasitic capacitance. This additional degree of freedom to fine-tune input matching is used in our design to enhance S_{11} at 1.9GHz. Alternative choices of L_{EQ} can enhance S_{11} at higher frequency, but to a lesser extent.

It can be shown that the noise factor is approximately

$$F \cong 1+\frac{r_t}{R_o}+\frac{R_o}{R_F}+K_1\frac{f_{-3dB}}{f_t} \cong 1+\frac{r_t}{R_o}+\frac{R_o}{R_F}+2\frac{f_{-3dB}}{f_t}. \quad (3)$$

Here, r_t is the sum of all resistors around the input loop including interconnect metal and vias, gate, and source resistance. R_o is the generator resistance. Some portion of the non-quasi-static charging resistance also has noise (h-parameter noise representation), but this is typically small compared to other components in 90nm technology, particularly since it is filtered by gate-source overlap capacitance. K_1, typically ~2, is a factor that captures enhanced channel noise, and noise from R_B, R_L, and M_2. C_F is used to control peaking and also plays some role in S_{11}.

From (2), it is seen that a high f_t and large R_F are desirable for low noise figure. Therefore, a scaled technology with a high f_t contributes to a low noise figure to the extent that r_t is not too large. A large R_F requires high gain, and this trades-off with linearity as the gain of M_1 causes M_2 to be driven by a relatively large signal. The mid-band loop gain of the circuit is

$$T \cong A_v\frac{R_o}{R_f} \cong 1. \quad (4)$$

Equation (4) is set by (1) to achieve a good input match. This small amount of feedback linearizes the LNA. At high frequencies, the loop gain decreases, resulting in degraded IIP$_3$.

The LNA was fabricated in two 90nm processes. One process is RF enhanced with a high resistivity epi/substrate, metal-insulator-metal (MIM) capacitors and precision poly resistors. The other is a digital process with low epi/substrate resistivity. Although MIM capacitors are available, inter-digitated metal capacitors are used. The circuit was tested with ground-signal-ground probes and an on-chip 50Ω driver. The driver is a modified super source-follower with a series pad output resistor as shown in Figure 11.5.2. The driver bandwidth is 10GHz and, at midband, S_{21} is -7dB and S_{22} is less than -20dB. The driver performance was measured and de-embedded for the measurements presented in Figure 11.5.3. We observe that at 5GHz, S_{11} is -13dB, voltage gain is 25dB, NF is 2dB, and IIP$_3$ is -14dBm for the RF enhanced process. The performance for the digital process is somewhat worse, except for IIP$_3$. Much of the reduction in performance for the digital process is due to modeling and extraction errors for the poly resistors in this process. The resistors that were fabricated are ~15% lower than the designed value. The low-resistivity substrate may also play some role.

Figures 11.5.4 and 11.5.5 show the impact of R_F, C_F and C_{PFB} on circuit performance. It was found that these parameters have negligible effect on linearity, and varying R_F by ±12.5% will change the noise figure by ∓0.1dB. Figure 11.5.6 is a table comparing our reported performance to other published data. The power is somewhat high but could be lowered, particularly if less gain and/or bandwidth are required. Note the power in $M4$ would typically be associated with the mixer in a receiver, and is 6.8mW in our design. Figure 11.5.7 is a micrograph of one of the LNAs and output driver.

Acknowledgement:
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References:
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[2] E. Duvivier, et al., "A Fully Integrated Zero-IF Transceiver for GSM-GPRS Quad-Band Application," *IEEE J. Solid-State Circuits,* vol. 38, pp. 2249-2257, Dec., 2003.
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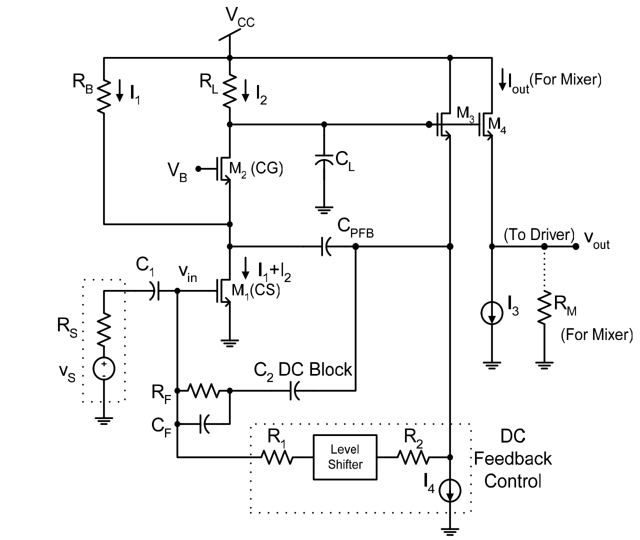

Figure 11.5.1: Simplified LNA schematic diagram.

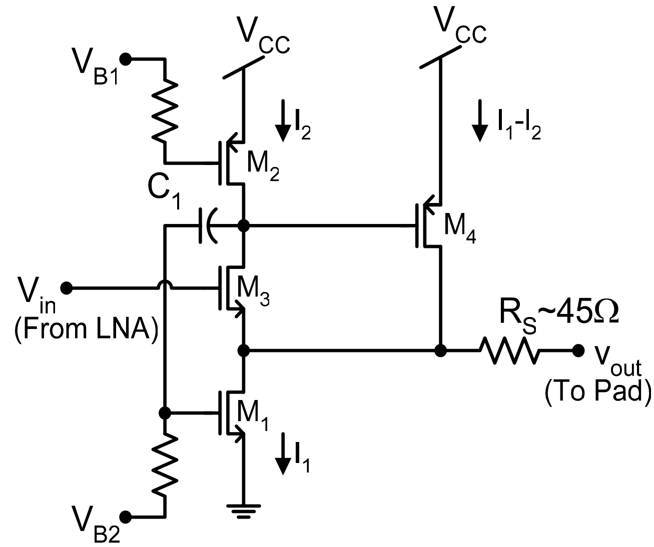

Figure 11.5.2: Simplified driver schematic diagram.

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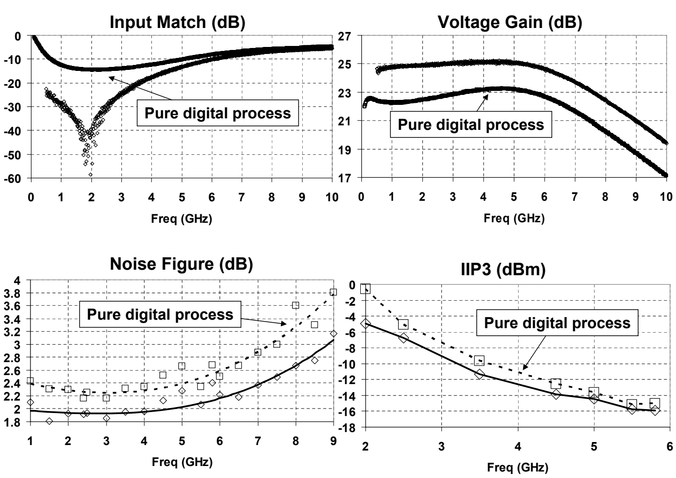

Figure 11.5.3: Measurement.

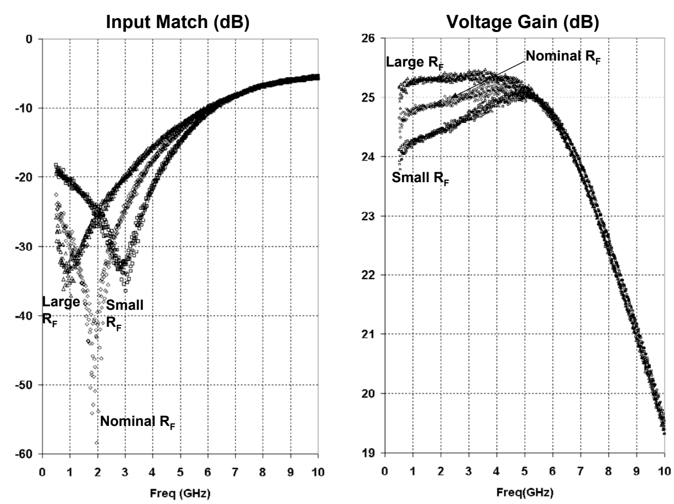

Figure 11.5.4: Effect of R_F.

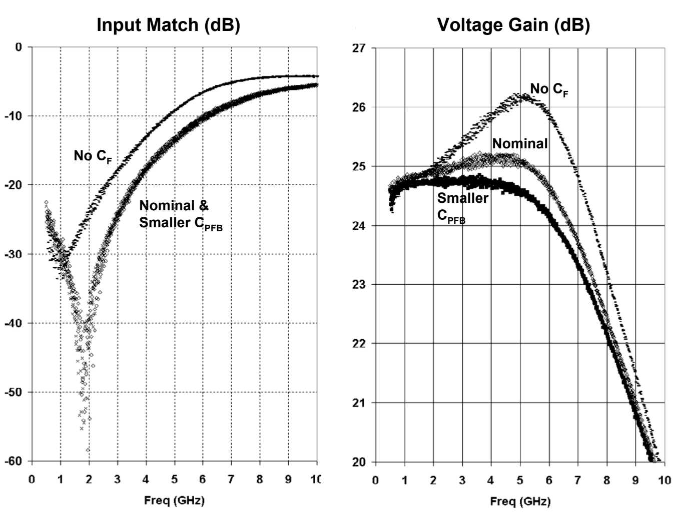

Figure 11.5.5: Effect of C_{PFB} and C_F.

Source	Process	Freq (GHz)	Gain (dB)	NF (dB)	OIP3 (dBm)	Supply (V)	Power (mW)	Active Area (μmxμm)
This Work	90nm CMOS	0.5-8.2	25	1.9-2.6	21@ 2GHz 8.8@5.8GHz	2.7	42	~0.025
JSSC 2005 pp. 1434	90nm CMOS	5.5	13.3	2.9	10.3	1.2	9.72	~0.455
JSSC 2005 pp. 726	180nm CMOS	5.2	16.5	1.11	12.5	1.8	12.4	~0.22
JSSC 2005 pp. 544	180nm CMOS	2-4.6	9.8	2.3	2.8	1.8	12.6	0.9
ISSCC 2005 pp. 534	180nm CMOS	5.8	9.4	2.5	2.2	1.8	3.4	~0.28
JSSC 2004 pp. 275	250nm CMOS	0.2-1.6	13.7	2-2.4	13.7	2.5	35	~0.075
JSSC 2004 pp. 2269	180nm SiGe	3-10	21	2.5-4.2	15.5 @3.5GHz 20 @5.5GHz	3	30	~0.7
JSSC 2004 pp. 2259	180nm CMOS	2.3-9.2	9.3	4	-6.7	1.8	9	~0.66

Figure 11.5.6: Performance summary and comparison.

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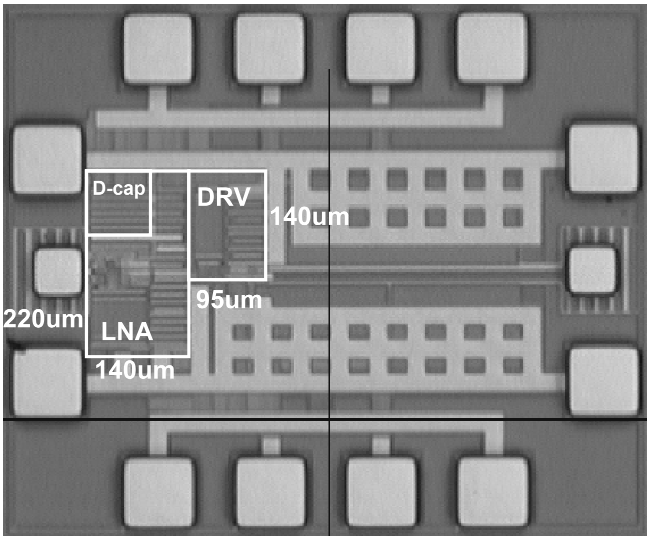

Figure 11.5.7: Chip microraph.